A New Cascaded Multilevel Inverter with Minimal Number of Switches

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Abstract: In recent technologies the multilevel inverters are exceptionally used in moderate and significant power applications considering their eminent operation characteristics. Primarily, the operating level of MLI's is subjected to number of levels generated in output voltage. Basically, the topologies of multilevel inverter are categorized as diode clamped, cascaded H-Bridge & flying capacitor, on comparing performance characteristics CMLI is preferred because of its standardized characteristics. However the conventional CMLI has considerable defects comparatively employs a sole DC source and requires the larger number of switching devices. Likely effects will boosted when there is increment in number of levels. But in this particular article, an advanced elementary block is recommended for obtaining more number of output levels together with fewer number of switching components. For acquiring the required number of output levels, altogether cascading the considerable elementary blocks in series. In addition to that the proposed MLI design has proficiency to generate only positive voltage levels. Apart from +ve levels to generate –ve levels, a unique H- bridge circuit is employed. Considering the amplitude of DC source four distinct principles are designed to obtain the required number of output levels. By comparing the proposed CHBMLI with the conventional CMLI, the proposed algorithm has superlative design with minimal operation of driver circuits, DC voltage sources and power switches. The designed algorithm is simulated in MATLAB / SIMULINK.

Keywords: Multilevel inverters, CHBMLI and CMLI.

I. INTRODUCTION

Multilevel Inverters (MLI's) has grabbed significant attention in power industry, as MLI's are predominately operating in moderate and greater power applications likely UPS, large induction motor drives, HVDC and FACTS transmission systems etc., [1-6] MLI's can comfortably generates the required output voltage levels using only single or number of input DC sources. .

Generated output waveform shape depends on number of output levels. Comparing with the basic 2 level voltage source inverter, MLI's are mostly preferred because of its performance like lesser voltage stress, minimized THD and reduced switching losses. Based on number of input DC sources these MLI's are categorized into different topologies, namely Diode Clampled Multi Level Inverter (DCMLI), Flying Capacitor Multi Level Inverter (FCMLI) and Cascaded H- Bridge Multi Level Inverter (CMLI). Among the three topologies CMLI's are mostly preferred because of its simplicity, modularity, doesn't require any clamping diodes and reliability

Further CMLI are categorized as symmetrical CMLI's & asymmetrical CMLI's, These CMLI's are differentiated by magnitudes of input DC sources. Hence the magnitudes of DC sources are identical in case of symmetrical CMLI where as for asymmetrical CMLI's the magnitudes of DC sources are different. The number of output levels generated more in asymmetrical CMLI than that of symmetrical CMLI. Foremost the asymmetrical CMLI's are apt for PV applications. However in asymmetrical CMLIs switching components has distinct ratings.

This article demonstrates both symmetrical and asymmetrical arrangements. The designed CMLI has ability to operate in symmetrical as well as asymmetrical arrangement. Articles [13]-[19] demonstrate distinct CMLI topologies performed as symmetrical configuration. On comparing with the proposed topology, few standard topologies demonstrated in these articles comprise DC sources, diodes and high number of switching elements.

At present an advanced elementary block is designed to generate greater number of output levels accompanied by fewer number of switching elements. For acquiring the required number of output levels, altogether cascading the considerable elementary blocks in series. In addition to that the proposed MLI design has proficiency to generate only positive voltage levels. Apart from +ve levels to generate –ve levels, a unique H- bridge circuit is employed. Considering the amplitude of DC source four distinct principles are designed to obtain the required number of output levels. The proposed CHBMLI has superlative design when compare to conventional CMLI.

Further sections of this article present the performance analysis: here section 2 demonstrates the proposed topography. Section 3 demonstrates the comparative analysis proposed CHBMLI with the conventional CMLI. Section 4 presents the analysis of proposed technologies. Likely next section conclude following with the simulation analysis.

II. PROPOSED TOPOLOGY

The proposed elementary block comprises of three DC voltage sources and five switching components cascaded according to fig. 1. This designed fundamental block generates 3 positive levels essentially 0, (V_1 + V_3), (V_1 + V_2 + V_3) and no negative voltage levels are generated at output. As elementary block comprises of five switching components, their status is together tabulated in table I. For acquiring the required number of output levels, altogether cascading the considerable elementary blocks in series.

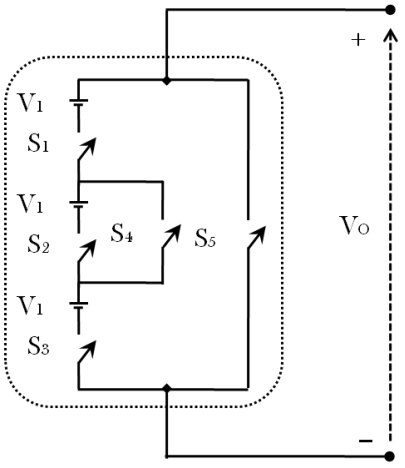


Fig.1 Elementary Block

Table I. Switching Pattern for Proposed Basic Unit

No of levels	Switching state					V_0
	S_1	S_2	S_3	S_4	S_5	
1	0	0	0	0	1	0
2	1	0	1	1	0	V_1 + V_3
3	1	1	1	0	0	V_1+V_2+V_3

The designed architecture is unable to generate V_1 level. To obtain the missing output levels (assuming the amplitude of $V_1 = V_{dc}$ i.e., same as minimum output level) the secondary unit is cascaded in series to fundamental block. This secondary unit comprises the switching components (S_1, S_2) and one DC voltage source which is cascaded in series with fundamental block, the conjunction of fundamental block and secondary unit represents the MLI structure which is displayed as fig. 2. The derived output voltage v_o of fundamental block and secondary unit is represented as:

$$V_O(t) = V_{0,1}(t) + V_{0,2}(t) + V_{0,3}(t) + \ldots\ldots\ldots\ldots + V_{0,n}(t) + V_1(t) \qquad (1)$$

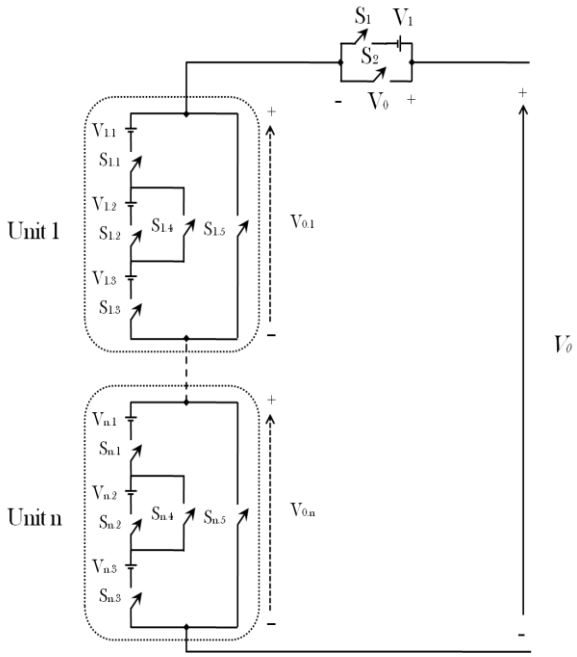


Fig.2 Proposed MLI Structure

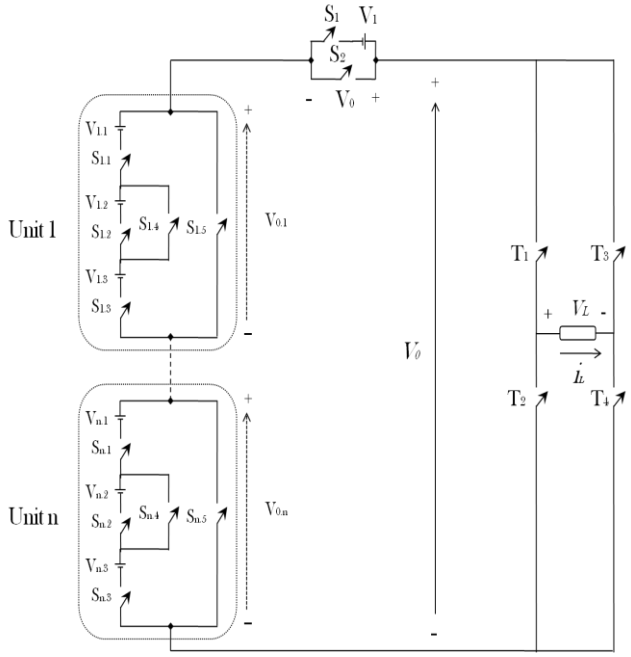


Fig.3 Proposed CHBMLI Structure

Table II. Generated Output Voltage Based on the States Power Switches

Generated output Voltage (vo)	S_1	S_2	$S_{1,1}$	$S_{1,2}$	$S_{1,3}$	$S_{1,4}$	$S_{1,5}$	$S_{2,1}$	$S_{2,2}$	$S_{2,3}$	$S_{2,4}$	$S_{2,5}$	|…	$S_{n,1}$	$S_{n,2}$	$S_{n,3}$	$S_{n,4}$	$S_{n,5}$
0	0	1	0	0	0	0	1	0	0	0	0	1	…	0	0	0	0	1
V_1	0	0	0	0	0	0	1	0	0	0	0	1	…	0	0	0	0	1
$V_{1,1}+V_{1,3}$	0	1	1	0	1	1	0	0	0	0	0	1	…	0	0	0	0	1
$V_{1.1}+V_{1.2}+V_{1.3}$	0	1	1	1	1	0	0	0	0	0	0	1	…	0	0	0	0	1
$V_{2,1}+V_{2,3}$	0	1	0	0	0	0	1	1	0	1	1	0	…	0	0	0	0	1
$V_{2,1}+V_{2,2}+V_{2,3}$	0	1	0	0	0	0	1	1	1	1	0	0	…	0	0	0	0	1
$V_{1,1}+V_{2,1}+V_{3,1}+V_{1,2}+V_{3,2}$	0	1	1	1	1	0	0	1	0	1	0	0	…	0	0	0	0	1
$V_{1,1}+V_{2,1}+V_{3,1}+V_{1,2}+V_{2,2}+V_{3,2}$	0	1	1	1	1	0	0	1	1	1	0	0	…	0	0	0	0	1
……	…..	…..	….	….	…	….	…	…	….	…	…	…	…	….	….	…	….	….
$\sum V_{j,1}+V_{j,2}+V_{j,3}$ For j=1,2,3,….n	0	1	1	1	1	0	0	1	1	1	0	0	...	0	0	0	0	1
$V_1+\sum V_{j,1}+V_{j,2}+V_{j,3}$ For j=1,2,3,….n	1	0	1	1	1	0	0	1	1	1	0	0	...	0	0	0	0	1

The switching component status and their corresponding output levels of MLI structure are tabulated in table II. This MLI structure generates only positive voltage levels. In order to attain both +ve and -ve levels, a single H-bridge circuit is used. This topology is stated as Proposed CHBMLI which is displayed as Fig.3.

Finally the number of switches "N_{switch}" and number of dc voltage sources "N_{source}" consider for the proposed new CHBMLI's are represented as:

$$N_{Switch} = 5n + 6 \qquad (2)$$

$$N_{Source} = 3n + 1 \quad (3)$$

Where n is the number of basic units connected in series.

This article demonstrates on both symmetrical and asymmetrical configurations. The proposed CMLI has ability to perform as symmetrical and asymmetrical configuration. Considering the amplitude of DC source four distinct principles are designed to obtain the required number of output levels. By comparing the proposed CHBMLI with the conventional CMLI, the proposed algorithm has superlative design. Number of output levels and their corresponding algorithms are tabulated in table III. The magnitudes of all DC voltage sources are identical in first algorithm but for remaining algorithms the magnitudes are not identical. Hence all proposed algorithms except the first are considered as an asymmetric CMLI's.

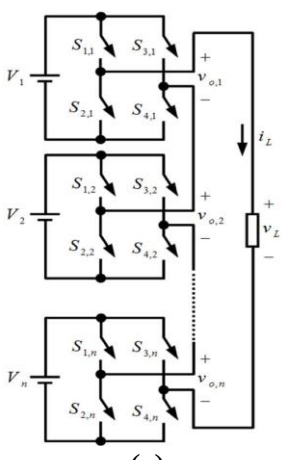
Table III. Proposed Algorithms and their Parameters, Where N= Number of Basic Units.

Proposed algorithm	**Magnitude of dc voltage sources**	**Number of levels** (m)	**Peak V_o**
First algorithm(P_1)	$V_{j,1}= V_{j,2}= V_{j,3} = V_{dc}$, For j=1,2,.....,n	6n+3	(3n+1) V_{dc}
Second algorithm(P_2)	$V_{1,1}= V_{1,2}= V_{1,3} = V_{dc}$ and $V_{j,1}= V_{j,2}= V_{j,3} = 2V_{dc}$ For j=2,3,.....,n	12n-3	(6n-2) V_{dc}
Third algorithm(P_3)	$V_{1,1} = V_{1,2}= V_{1,3} = V_{dc}$ $V_{j,1} = (1/3)V_{j,2} = V_{j,3} = (3^{j-2})V_{dc}$ for j=2,3,.....,n	$5(3^{n-1})+4$	$[(5(3^{n-1})+3)/2]$ V_{dc}
Fourth algorithm(P4)	$V_{j,1} = 0.5\ V_{j,2} = V_{j,3} = (2^{j-1})V_{dc}$ For j=1,2,.....,n	$2^{n+3}-5$	$(2^{n+2}-3)$ V_{dc}

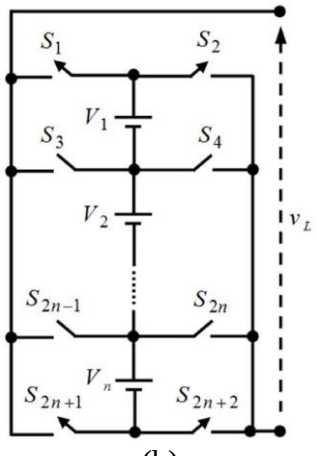
Moreover, based on equations of maximum output voltage and its amplitude, Asymmetrical CMLI produces more no. of output levels that of symmetrical CMLI by considering identical no. of switching elements and DC voltage sources.

III. COMPARING THE PROPOSED TOPOLOGY WITH CONVENTIONAL TOPOLOGIES

Major purpose of suggested CHBMLI is to produce more no. of output steps with minimal no. of switches. . Comparison is accomplished between the suggested CHBMLI and traditional CMLIs in terms of driver circuits, power switches & dc voltage sources.



(a)



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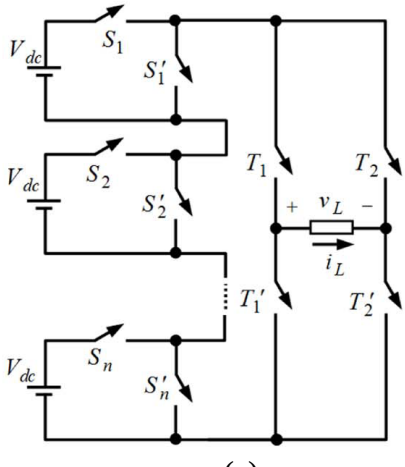

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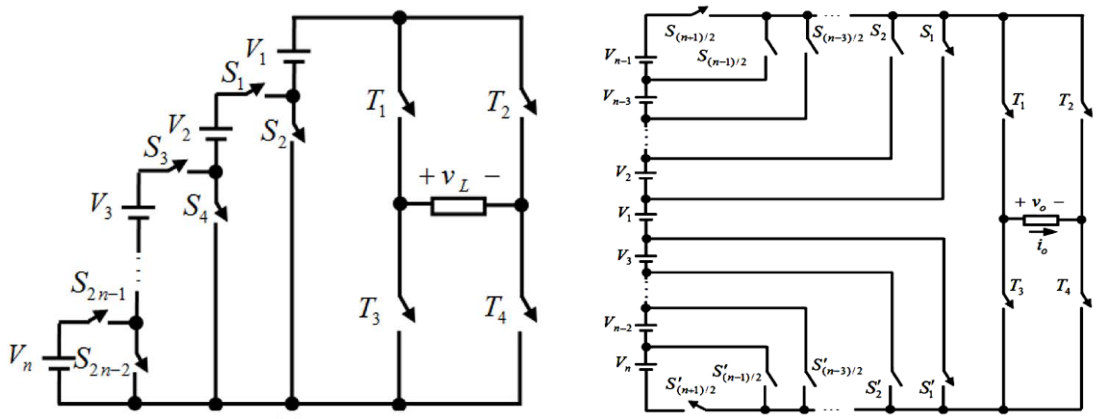

(d) (e)

Fig.4 Different CMLI Topologies (a) Reported in [14], (b) Reported in [15], (c) Reported in [16], (d) Reported in [17], (e) Reported in [18].

In this comparison, different algorithms for proposed CHBMLI are represented by P_1-P_4, respectively and different traditional CMLI's published in [14]-[18] are considered. The above mentioned CMLI's entire are indicated Fig. 4.

Table IV. Components Required Comparison between Conventional CMLI and Proposed CHBMLI

Converter Type	**Conventional CMLI published**					**Proposed CHBMLI with algorithms**			
Parameter	[14]	[15]	[16]	[17]	[18]	P1	P2	P3	P4
Main Switches Count	$2(m-1)$	$(m+1)$	$(m+3)$	$(m+1)$	$(m+3)$	$5\left(\frac{(m-3)}{6}\right)+6$	$5\left(\frac{(m-3)}{12}\right)+6$	$5\left[\frac{\left(\log\frac{3(m-4)}{5}\right)}{\log 3}\right]+6$	$5\left[\frac{\left(\log(\frac{m+5}{8}\right)}{\log 2}\right]+6$
No. of Sources	$\frac{(m-1)}{2}$	$\frac{(m-1)}{2}$	$\frac{(m-1)}{2}$	$\frac{(m-1)}{2}$	$\frac{(m-1)}{2}$	$\left(\frac{(m-3)}{2}\right)+1$	$\left(\frac{(m-3)}{4}\right)+1$	$3\left[\frac{\left(\log\frac{3(m-4)}{5}\right)}{\log 3}\right]+1$	$3\left[\frac{\left(\log(\frac{m+5}{8}\right)}{\log 2}\right]+1$

The table IV illustrates comparison of components requirement of a single phase proposed verses conventional topology to produce "m" level of output voltage.

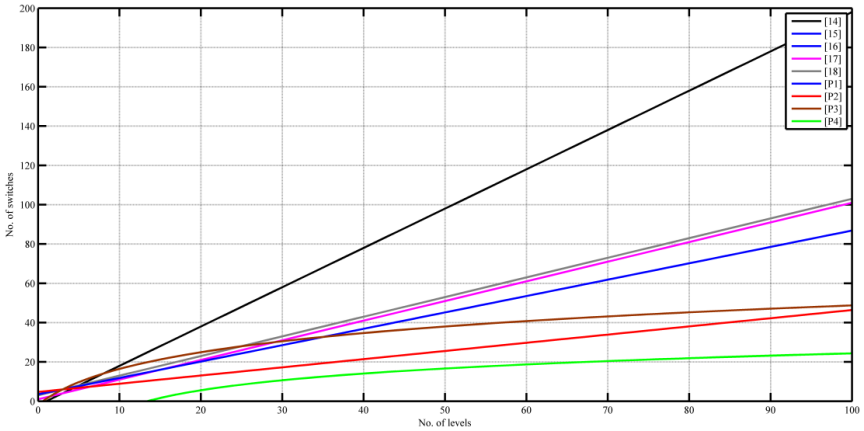

Fig.5 Number of Switches Required for m Level

Based on table IV, Fig. 6 clearly compares the no. of DC voltage sources of proposed topology to traditional CMLIs, It is noticeable that the no. of DC voltage sources required for developed inverter

are lesser than that of other existing inverters. This variation will be higher on considering the fourth proposed algorithm.

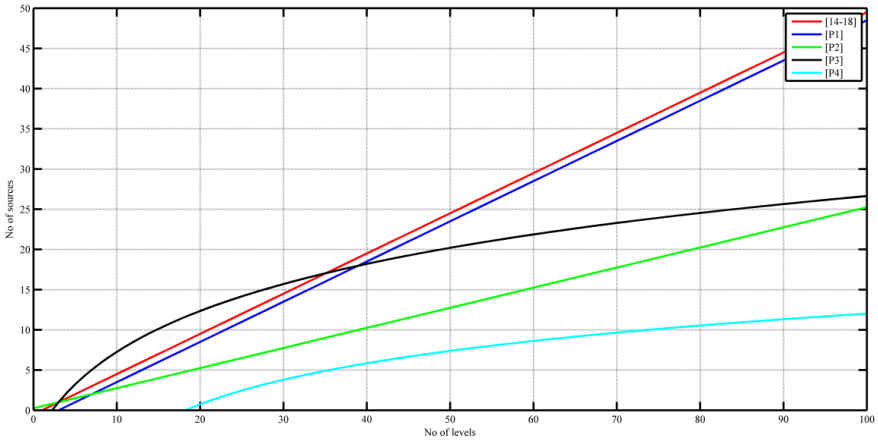

Fig.6 Number of Sources Required for m Level

IV. MODULATION TECHNIQUES

In major industrial applications, the output voltages of inverters need to be varied. The appearance of MLI's depends on switching schemes used for developing PWM signals.

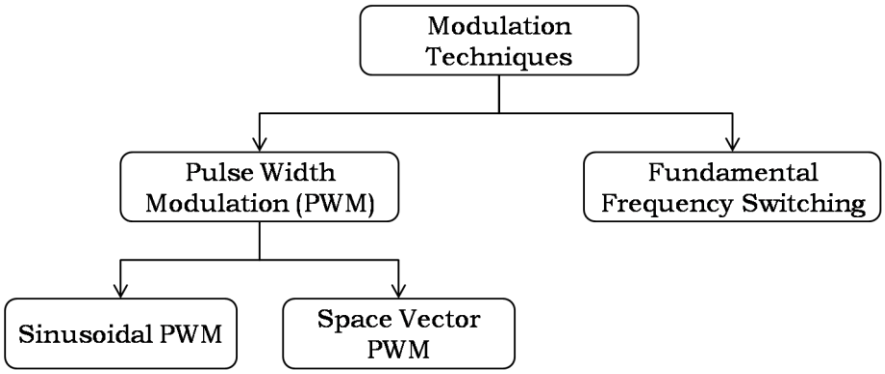

Fig.7 Types of PWM Schemes

Fig.7 shows different modulation schemes. Out of these spwm scheme is more preferrable for MLIs due to its merits. Level shift and phase shift PWM schemes are another classification of SPWM scheme. In this paper the different level shifted PWM techniques are considered likely In Phase Disposition (IPD), Phase Opposition Disposition (POD) and Alternative Phase Opposition Disposition (APOD) are considered.

V. SIMULATION RESULTS

The implementation of proposed CHBMLI with two elementary blocks by different level shift SPWM schemes established through MATLAB simulation. The suggested CMLI is able to operate both symmetrical and asymmetrical configuration. This script reveals four different algorithms based on amplitudes of DC sources for achieving desired no. of output levels. The simulation results are validated for four different algorithms.

The simulated values are as follows: Input voltage 20V, Carrier frequency 100 kHz, Reference frequency 50 Hz, Modulation Index = 0.96. Table V shows the % of THD obtained with different carrier distribution with proposed algorithm. It is observed that the % of THD obtained with P4 algorithm is as per IEEE standards.

Table V. % of THD Obtained by Different Algorithm

	P1	P2	P3	P4
Technique	**% THD**			
APOD	8.80	5.96	6.66	4.51
IPD	8.92	5.95	6.66	4.51
POD	8.81	5.95	6.65	4.54

From fig.8 to fig.10 shows fundamental output voltage and % THD for P1 algorithm using different level shift modulation schemes.

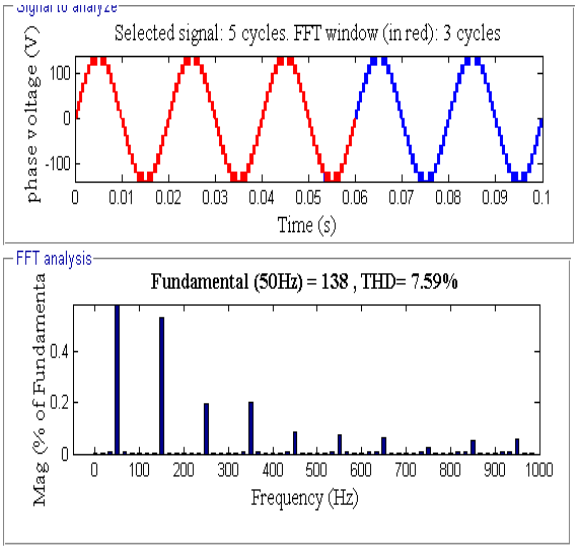

Fig.8 P1 Algorithm Output Voltage using APOD-PWM

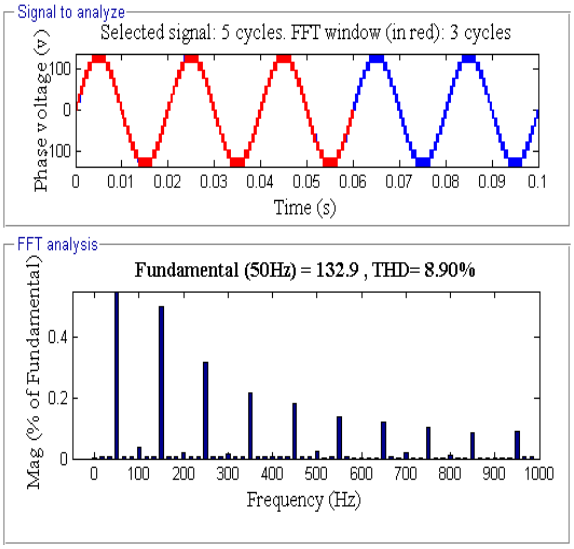

Fig.9 P1 Algorithm Output Voltage using PD-PWM

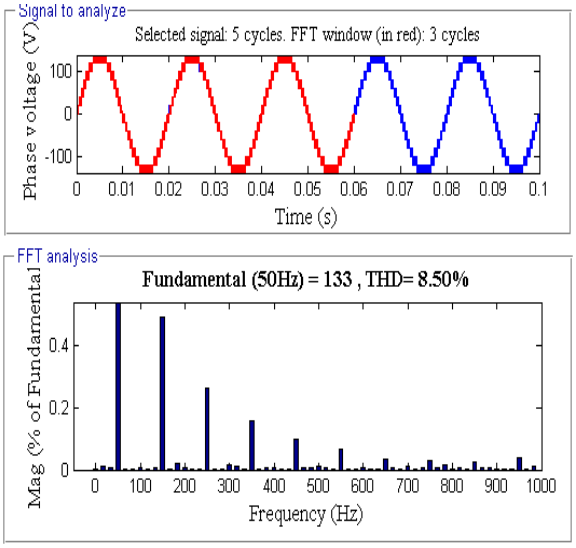

Fig.10 P1 Algorithm Output Voltage using POD-PWM

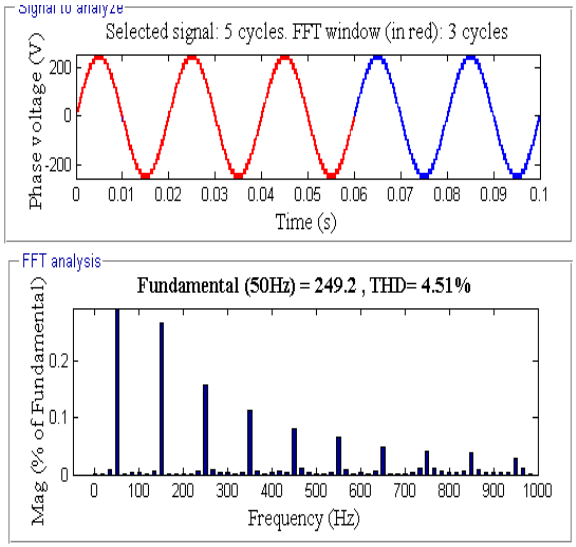

Fig.11 P4 Algorithm Output Voltage using APOD-PWM

From fig.11 to fig.13 shows fundamental output voltage and % THD for P4 algorithm using different level shift modulation schemes

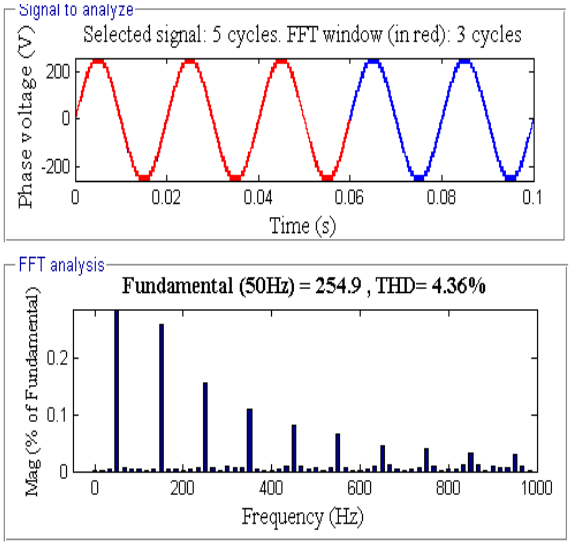

Fig.12 P4 Algorithm Output Voltage using PD-PWM

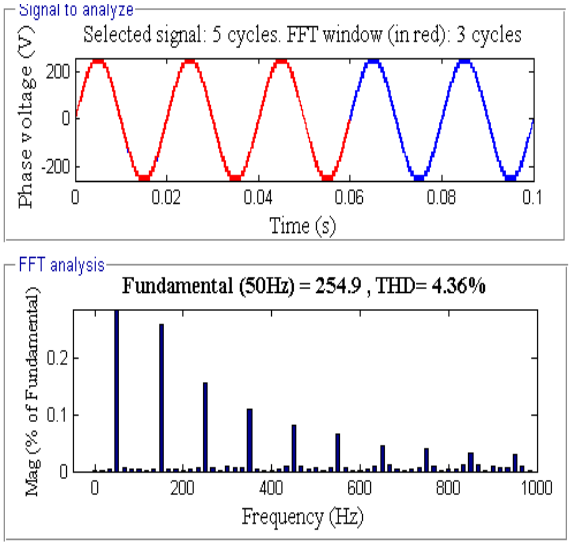

Fig.13 P4 Algorithm Output Voltage using POD-PWM

VI. CONCLUSION

Comparison is accomplished between the Proposed CHBMLI and the conventional CMLI. Utilization of no. of switches and DC sources are lower in Proposed CHBMLI compare to earlier CMLIs discussed in this script. Fourth algorithm gives higher output voltage and lower THD than remaining algorithms with same no. of switches and driver circuits. It is conclusive that the suggested model is finest in terms of lesser usage of switches, driver circuits, and DC sources. Suggested CHBMLI can be designed for real time applications due to its features.

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